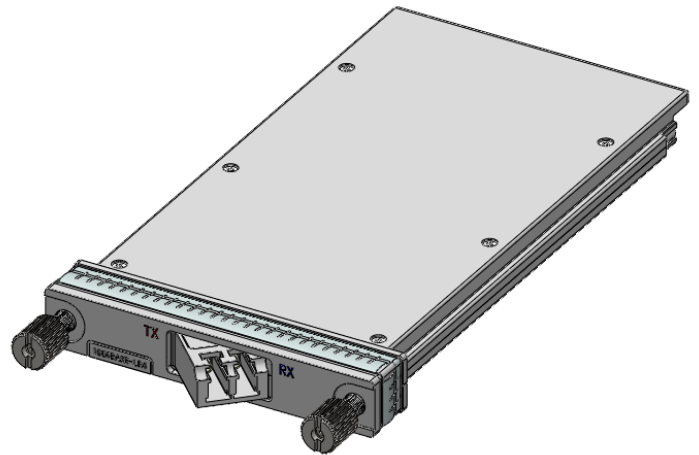


## EOLC-161HG-40-LA Series

Single-Mode OTU4 4I1-9C1F CFP Transceiver  
 Single-Mode 100GBASE-ER4 CFP Transceiver  
 RoHS6 Compliant

### Features

- ◆ Supports 103Gbps and 112Gbps aggregate bit rates
- ◆ Single 3.3V Power Supply and Power dissipation < 16W
- ◆ Up to 40km transmission on SMF
- ◆ Hot-Pluggable CFP Footprint Duplex LC Connector Interface
- ◆ Class 1 FDA and IEC60825-1 Laser Safety Compliant
- ◆ RoHS6 Compliant
- ◆ Operating Case Temperature Standard: 0°C~+70°C
- ◆ Compliant with CFP MSA Specification
- ◆ MDIO interface with integrated Digital Diagnostic Monitoring
- ◆ CAUI electrical interface



### Applications

- ◆ OTU4 4I1-9C1F
- ◆ 100GBASE-ER4

### Ordering Information

Part No.	Data Rate	Fiber	Distance *(Note2)	Interface	Temp.	DDMI
EOLC-161HG-40-LA*(Note1)	112Gbps (Note3)	SMF	40km	LC	Standard	Yes

Note1: Standard version

Note2: 40km with 9/125µm SMF

Note3: can change to 103Gbps rate through MDIO.

\*The product image only for reference purpose.

## Regulatory Compliance\*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

\*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Eoptolink.

## Absolute Maximum Ratings\*<sup>Note4</sup>

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T <sub>s</sub>	-40	+85	°C
Case Temperature	T <sub>c</sub>	-5	+75	°C
Supply Voltage	V <sub>cc</sub>	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

Note4: Exceeding any one of these values may destroy the device immediately.

## Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T <sub>c</sub> EOLC-161HG-40-LA	0		+70	°C
Power Supply Voltage	V <sub>cc</sub>	3.2	3.3	3.4	V
Power Supply Current	I <sub>cc</sub>		2700		mA

## Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
<b>Transmitter</b>						
Input Amplitude (Differential)	V <sub>in</sub>			1050	mVpp	AC coupled inputs* <sup>(Note7)</sup>
Input Impedance (Differential)	Z <sub>in</sub>	80	100	120	ohms	R <sub>in</sub> > 100 kohms @ DC
<b>Receiver</b>						
Output Amplitude (Differential)	V <sub>out</sub>	360		770	mVpp	AC coupled outputs* <sup>(Note7)</sup>
Output Impedance (Differential)	Z <sub>out</sub>	80	100	120	ohms	
Output Rise/Fall Time	t <sub>r</sub> /t <sub>f</sub>	24			ps	20%~80%

### MDIO Interface Specifications

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Input Voltage	V <sub>IH</sub>	0.84		1.5	V	
	V <sub>IL</sub>	-0.3		0.36	V	
Input Leak current	I <sub>IN</sub>	-100		100	uA	
Output Voltage	V <sub>OH</sub>	1.0		1.5	V	
	V <sub>OL</sub>	-0.3		0.2	V	
Input Capacitance	C <sub>I</sub>			10	pF	
Input MDC Clock	f <sub>MDC</sub>	0.1		4	MHz	
MDC Clock Period	T <sub>MDC</sub>	250		10000	ns	
MDIO Hold Time	T <sub>hold</sub>	10			ns	
MDIO Setup Time	T <sub>setup</sub>	10			ns	
GLB_ALM	T <sub>glb_alm_ass</sub>			150	ms	
	T <sub>glb_alm_dea</sub>			150	ms	

### Optical and Electrical Characteristics

#### OTU4 4I1-9C1F Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Transmitter</b>					
Signaling Speed per Lane	BR <sub>AVE</sub>		27.95		Gbps
Data rate variation		-20		20	ppm
Lane_0 Center Wavelength	λ <sub>C0</sub>	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ <sub>C1</sub>	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ <sub>C2</sub>	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ <sub>C3</sub>	1308.09	1309.14	1310.19	nm
Total Average Output Power <sup>*(Note5, Note6)</sup>	P <sub>O1</sub>	-		8.9	dBm
Average Launch Power per Lane <sup>*(Note6)</sup>	P <sub>each1</sub>	-2.7		2.9	dBm
Maximum channel power difference				3.6	dB
Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Extinction Ratio <sup>*(Note6)</sup>	ER <sub>1</sub>	8			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} <sup>*(Note6)</sup>			G.959.1 Compliant		
TX Disable Assert Time	t <sub>off</sub>			100	us
<b>Receiver</b>					
Signaling Speed per Lane	BR <sub>AVE</sub>		27.95		Gbps
Data rate variation		-20		20	ppm
Lane_0 Center Wavelength	λ <sub>C0</sub>	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ <sub>C1</sub>	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ <sub>C2</sub>	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ <sub>C3</sub>	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane <sup>*(Note9)</sup>	R <sub>pow1</sub>	-20.7		4.5	dBm

Maximum mean total input power				10.5	dBm
Equivalent Sensitivity per Lane <sup>*(Note11)</sup>	$P_{min1}$			-23.2	dBm
Maximum channel power difference				4.5	dB

## 100GBASE-ER4 Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Transmitter</b>					
Signaling Speed per Lane	$BR_{AVE}$		25.78		Gbps
Data rate variation		-100		100	ppm
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm
Total Average Output Power <sup>*(Note5, Note8)</sup>	$P_{O2}$	-		8.9	dBm
Average Launch Power per Lane <sup>*(Note8)</sup>	$P_{each2}$	-2.9		2.9	dBm
Optical modulation amplitude	OMA	0.1		4.5	dB
Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Extinction Ratio <sup>*(Note8)</sup>	$ER_2$	8			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} <sup>*(Note8)</sup>		IEEE802.3ba-2010 Compliant			
TX Disable Assert Time	$t_{off}$			100	us
<b>Receiver</b>					
Signaling Speed per Lane	$BR_{AVE}$		25.78		Gbps
Data rate variation		-100		100	ppm
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane <sup>*(Note10)</sup>	$R_{pow2}$	-20.9		4.5	dBm
Receiver power(OMA)	$P_{ovl}$			4.5	dBm
Difference in receive power between any two lanes(Average and OMA)				4.5	dB
Receive Sensitivity(OMA) per Lane <sup>*(Note12)</sup>	$P_{min2}$			-21.4	dBm
Stressed Sensitivity(OMA) per lane	SRS			-17.9	dBm

Note5: Output is coupled into a 9/125 $\mu$ m single-mode fiber.

Note6: Filtered, measured with a PRBS  $2^{31}-1$  test pattern @27.95Gbps

Note7: High speed I/O, internally AC coupled.

Note8: Filtered, measured with a PRBS  $2^{31}-1$  test pattern @25.78Gbps

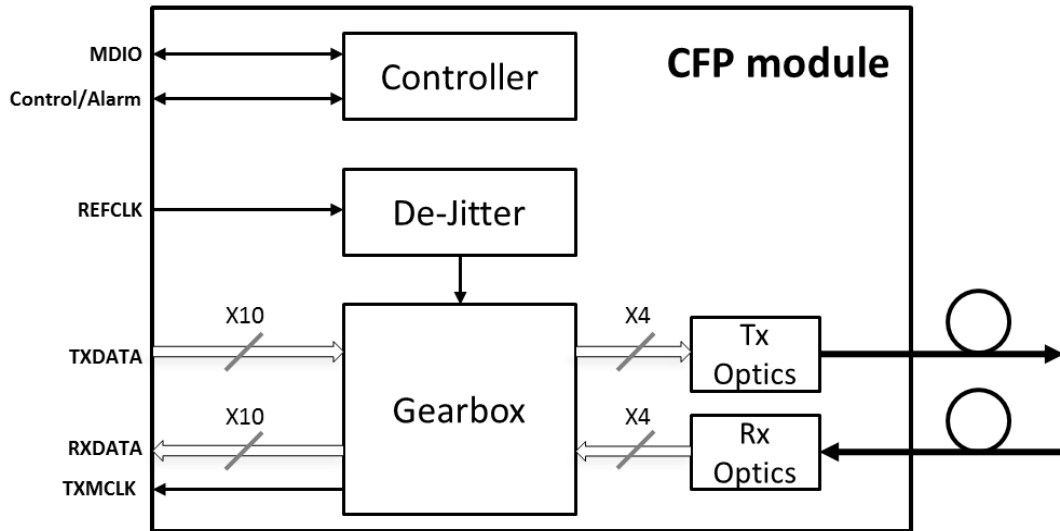
Note9: CFP transceiver works in OTU4 411-9C1F mode.

Note10: CFP transceiver works in 100GBASE-ER4 mode.

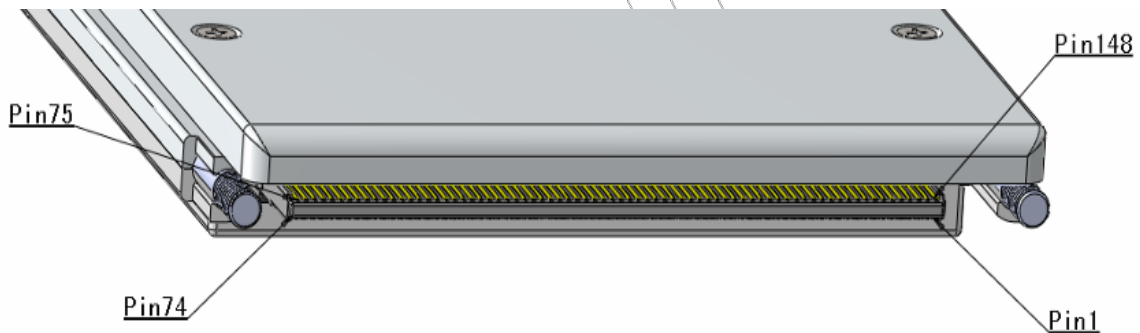
Note11: Measured at BER less than  $1E-12$ , with a  $2^{31}-1$  PRBS@27.95Gbps (W/ FEC).

Note12: Measured at BER less than  $1E-12$ , with a  $2^{31}-1$  PRBS@25.78Gbps.

## Functional Description of Transceiver



## CFP Transceiver Electrical Pad Layout



## Pin Function Definitions

CFP Top Row			
148	GND	111	GND
147	REFCLKn	110	N.C.
146	REFCLKp	109	N.C.
145	GND	108	GND
144	N.C.	107	RX9n
143	N.C.	106	RX9p
142	GND	105	GND
141	TX9n	104	RX8n
140	TX9p	103	RX8p
139	GND	102	GND
138	TX8n	101	RX7n
137	TX8p	100	RX7p
136	GND	99	GND

CFP Bottom Row			
1	3.3V_GND	38	MOD_ABS
2	3.3V_GND	39	MOD_RSTn
3	3.3V_GND	40	RX_LOS
4	3.3V_GND	41	GLB_ALRMn
5	3.3V_GND	42	PRTADR4
6	3.3V	43	PRTADR3
7	3.3V	44	PRTADR2
8	3.3V	45	PRTADR1
9	3.3V	46	PRTADR0
10	3.3V	47	MDIO
11	3.3V	48	MDC
12	3.3V	49	GND
13	3.3V	50	VND_IO_F

135	TX7n	98	RX6n	14	3.3V	51	VND_IO_G
134	TX7p	97	RX6p	15	3.3V	52	GND
133	GND	96	GND	16	3.3V_GND	53	VND_IO_H
132	TX6n	95	RX5n	17	3.3V_GND	54	VND_IO_J
131	TX6p	94	RX5p	18	3.3V_GND	55	3.3V_GND
130	GND	93	GND	19	3.3V_GND	56	3.3V_GND
129	TX5n	92	RX4n	20	3.3V_GND	57	3.3V_GND
128	TX5p	91	RX4p	21	VND_IO_A	58	3.3V_GND
127	GND	90	GND	22	VND_IO_B	59	3.3V_GND
126	TX4n	89	RX3n	23	GND	60	3.3V
125	TX4p	88	RX3p	24	(TX_MCLKn)	61	3.3V
124	GND	87	GND	25	(TX_MCLKp)	62	3.3V
123	TX3n	86	RX2n	26	GND	63	3.3V
122	TX3p	85	RX2p	27	VND_IO_C	64	3.3V
121	GND	84	GND	28	VND_IO_D	65	3.3V
120	TX2n	83	RX1n	29	VND_IO_E	66	3.3V
119	TX2p	82	RX1p	30	PRG_CNTL1	67	3.3V
118	GND	81	GND	31	PRG_CNTL2	68	3.3V
117	TX1n	80	RX0n	32	PRG_CNTL3	69	3.3V
116	TX1p	79	RX0p	33	PRG_ALARM1	70	3.3V_GND
115	GND	78	GND	34	PRG_ALARM2	71	3.3V_GND
114	TX0n	77	(RX_MCLKn)	35	PRG_ALARM3	72	3.3V_GND
113	TX0p	76	(RX_MCLKp)	36	TX_DIS	73	3.3V_GND
112	GND	75	GND	37	MOD_LOPWR	74	3.3V_GND

### Bottom Row Pin Descriptions

Pin Num.	Name	Function	Notes
1	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
2	3.3V_GND		
3	3.3V_GND		
4	3.3V_GND		
5	3.3V_GND		
6	3.3V	3.3V Module Supply Voltage	3.3V ± 2.5%
7	3.3V		
8	3.3V		
9	3.3V		
10	3.3V		
11	3.3V		
12	3.3V		
13	3.3V		
14	3.3V		
15	3.3V		
16	3.3V_GND	Ground	3.3V Module Supply Ground, Internally

17	3.3V_GND		connected to Signal Ground
18	3.3V_GND		
19	3.3V_GND		
20	3.3V_GND		
21	VND_IO_A	I/O	Module Vendor I/O, NC
22	VND_IO_B	I/O	Module Vendor I/O, NC
23	GND	Ground	Signal Ground
24	TX_MCLKn	Tx Monitor Clock	Tx Monitor Clock Output
25	TX_MCLKp	O	
26	GND	Ground	Signal Ground
27	VND_IO_C	I/O	Module Vendor I/O, Must not connect at host board
28	VND_IO_D	I/O	Module Vendor I/O, Must not connect at host board
29	VND_IO_E	I/O	Module Vendor I/O, Must not connect at host board
30	PRG_CNTL1	I	LVCOMS
31	PRG_CNTL2	I	LVCOMS
32	PRG_CNTL3	I	LVCOMS
33	PRG_ALRM1	O	LVCOMS
34	PRG_ALRM2	O	LVCOMS
35	PRG_ALRM3	O	LVCOMS
36	TX_DIS	Transmitter Disable I	"1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPW R	Module Low Power Mode I	"1" or NC: module in low power (safe) mode, "0": power-on enabled
38	MOD_ABS	Module Absent O	"1" or NC: module absent, "0": module present
39	MOD_RSTn	Module Reset I	"0" resets the module, "1" or NC = module enabled
40	RX_LOS	Loss of Signal O	"1": low optical signal, "0": normal condition
41	GLB_ALRMn	Global Alarm O	"0": alarm condition in any MDIO Alarm register, "1": no alarm condition
42	PRTADR4	1.2V CMOS I	MDIO Physical Port address bit4
43	PRTADR3	1.2V CMOS I	MDIO Physical Port address bit3
44	PRTADR2	1.2V CMOS I	MDIO Physical Port address bit2

45	PRTADR1	1.2V CMOS I	MDIO Physical Port address bit1
46	PRTADR0	1.2V CMOS I	MDIO Physical Port address bit0
47	MDIO	1.2V CMOS I/O	Management Data I/O bi-directional data
48	MDC	1.2V CMOS I	Management Data Clock
49	GND	Ground	Signal Ground
50	VND_IO_F	I/O	Module Vendor I/O, Not Connected Internally
51	VND_IO_G	I/O	Module Vendor I/O, Not Connected Internally
52	GND	Ground	Signal Ground
53	VND_IO_H	I/O	Module Vendor I/O, Not Connected Internally
54	VND_IO_J	I/O	Module Vendor I/O, Not Connected Internally
55	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
56	3.3V_GND		
57	3.3V_GND		
58	3.3V_GND		
59	3.3V_GND		
60	3.3V	3.3V Module Supply Voltage	3.3V ± 2.5%
61	3.3V		
62	3.3V		
63	3.3V		
64	3.3V		
65	3.3V		
66	3.3V		
67	3.3V		
68	3.3V		
69	3.3V		
70	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
71	3.3V_GND		
72	3.3V_GND		
73	3.3V_GND		
74	3.3V_GND		

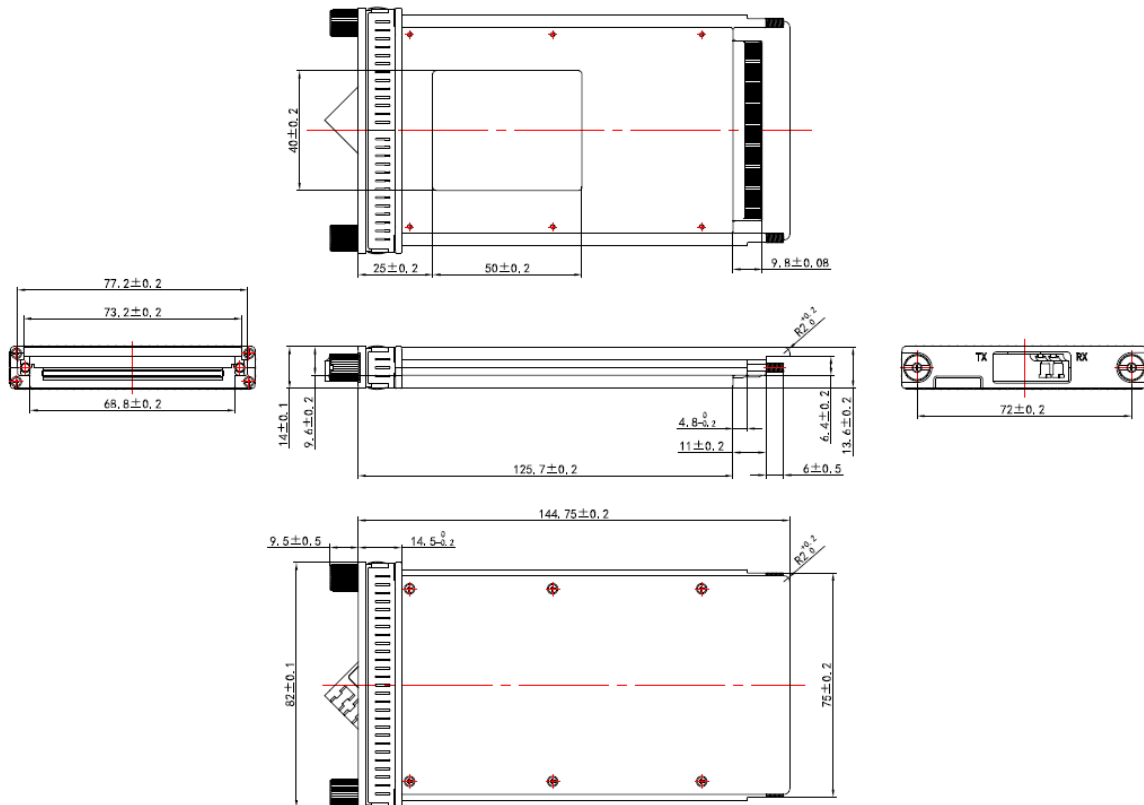


## Top Row Pin Descriptions

Pin Num.	Name	Function	Notes
148	GND	Ground	Signal Ground
147	REFCLKn	Reference Clock I	Reference Clock Input
146	REFCLKp		
145	GND	Ground	Signal Ground
144	N.C.		Not Connected Internally
143	N.C.		Not Connected Internally
142	GND	Ground	Signal Ground
141	TX9n	Lane 9 Tx Input I	
140	TX9p		
139	GND	Ground	Signal Ground
138	TX8n	Lane 8 Tx Input I	
137	TX8p		
136	GND	Ground	Signal Ground
135	TX7n	Lane 7 Tx Input I	
134	TX7p		
133	GND	Ground	Signal Ground
132	TX6n	Lane 6 Tx Input I	
131	TX6p		
130	GND	Ground	Signal Ground
129	TX5n	Lane 5 Tx Input I	
128	TX5p		
127	GND	Ground	Signal Ground
126	TX4n	Lane 4 Tx Input I	
125	TX4p		
124	GND	Ground	Signal Ground
123	TX3n	Lane 3 Tx Input I	
122	TX3p		
121	GND	Ground	Signal Ground
120	TX2n	Lane 2 Tx Input I	
119	TX2p		
118	GND	Ground	Signal Ground
117	TX1n	Lane 1 Tx Input I	
116	TX1p		
115	GND	Ground	Signal Ground
114	TX0n	Lane 0 Tx Input I	
113	TX0p		
112	GND	Ground	Signal Ground
111	GND	Ground	Signal Ground
110	N.C.		Not Connected Internally
109	N.C.		Not Connected Internally
108	GND	Ground	Signal Ground

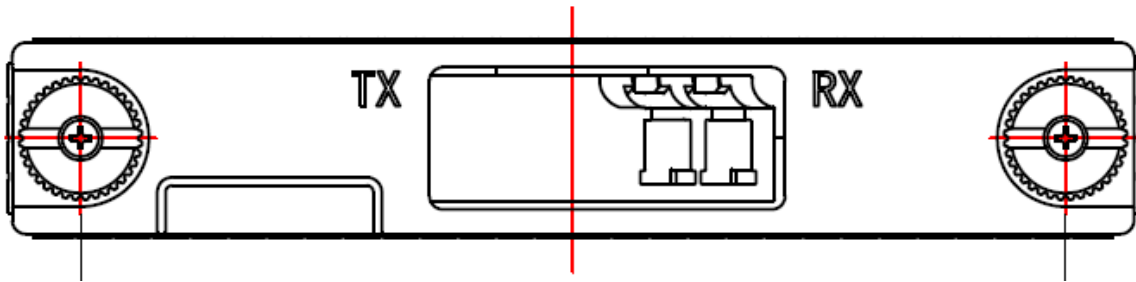
107	RX9n	Lane 9 Rx Output	
106	RX9p	O	
105	GND	Ground	Signal Ground
104	RX8n	Lane 8 Rx Output	
103	RX8p	O	
102	GND	Ground	Signal Ground
101	RX7n	Lane 7 Rx Output	
100	RX7p	O	
99	GND	Ground	Signal Ground
98	RX6n	Lane 6 Rx Output	
97	RX6p	O	
96	GND	Ground	Signal Ground
95	RX5n	Lane 5 Rx Output	
94	RX5p	O	
93	GND	Ground	Signal Ground
92	RX4n	Lane 4 Rx Output	
91	RX4p	O	
90	GND	Ground	Signal Ground
89	RX3n	Lane 3 Rx Output	
88	RX3p	O	
87	GND	Ground	Signal Ground
86	RX2n	Lane 2 Rx Output	
85	RX2p	O	
84	GND	Ground	Signal Ground
83	RX1n	Lane 1 Rx Output	
82	RX1p	O	
81	GND	Ground	Signal Ground
80	RX0n	Lane 0 Rx Output	
79	RX0p	O	
78	GND	Ground	Signal Ground
77	RX_MCLKn	Rx Monitor Clock	Not Connected Internally
76	RX_MCLKp	O	
75	GND	Ground	Signal Ground

### Mechanical Specifications



\*This 2D drawing only for reference, please check with Eoptolink before ordering.

### Laser Emission



### Obtaining Document

You can visit our website: <http://www.eoptolink.com>

Or contact Eoptolink Technology Inc., Ltd. listed at the end of the documentation to get the latest documents.

### Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Bob/Torres/Neal /Tony			Initial Version.	Jan 18, 2017

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