EOLC-161HG-80-AY

EOLC-161HG-80-BY

EOLC-161HG-80-CY

EOLC-161HG-80-DY

DWDM CFP Transceiver
RoHS6 Compliant

Features

- 10x10Gbps Transceiver
- Pluggable CFP module – compliant to existing CFP blade design
- 10x10 MSA standard compliant
- DWDM C-band 100Ghz grid
- Up to 1600ps/nm dispersion tolerance
- Power Consumption 20 Watt typical
- Integrated EDC and PA
- Up to 80km reach (with no external DCF and no external Optical Amplifier)
- Case operating temperature:
  Standard: 0~70℃

Applications

- Router interconnect
- Mesh, Ring and Point to point
- 100G client extension
- Low-cost / higher density 100G line interface
- High density 10 x 10G
- 10G XFP -> 100G 80km upgrade
- Metro, metro-access, core bypass

Ordering Information

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
EOLC-161HG-80-A/B/C/DY *(note1)	100Gbps	SMF	80km	LC	Standard	Yes

Note1: A/B/C/D refers to DWDM Group:

Code	DWDM Group
A	ITU C52-C61
B	ITU C41-C50
C	ITU C30-C39
D	ITU C19-C28

Note2: 80km with 9/125μm SMF
*The product image only for reference purpose.

DWDM Wavelength Assignment (100G series)

Parameter	Unit	Min	Typ	Max	Note
Channel Spacing	GHz		100		0.8nm
Wavelength accuracy	GHz	-12.5		+12.5	10x10 MSA Table 4-1
Channel No.	4 sub-bands in C-Band				ITU-T G.694.1
Band 1(C61 – C52)	1528.77 - 1535.82 nm				
Optical Central Wavelength λc [nm]	1528.77, 1529.55, 1530.33, 1531.12, 1531.90 1532.68, 1533.47, 1534.25, 1535.04, 1535.82				
Band 2 (C50-C41)	1537.40 - 1544.53 nm				
Optical Central Wavelength λc [nm]	1537.40, 1538.19, 1538.98, 1539.77, 1540.56 1541.35, 1542.14, 1542.94, 1543.73, 1544.53				
Band 3 (C39-C30)	1546.12 - 1553.33 nm				
Optical Central Wavelength λc [nm]	1546.12, 1546.92, 1547.72, 1548.5, 1549.32, 1550.12, 1550.92, 1551.72, 1552.52, 1553.33				
Band 4 (C28-C19)	1554.94 - 1562.23 nm				
Optical Central Wavelength λc [nm]	1554.94, 1555.75, 1556.55, 1557.36, 1558.17, 1558.98, 1559.79, 1560.61,1561.42, 1562.23				

Regulatory Compliance*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013

FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Eoptolink.

Absolute Maximum Ratings*Note3

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	℃
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

Note3: Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	EOLC-161HG-80-A/B/C/DY	0		+70	℃
Power Supply Voltage	Vcc		3.15	3.3	3.45	V
Power Comsumption	P			20	24	W
Supported Bit Rate	Gbe			103.125		Gbps
	OTU3			107.09		
	OTU4			111.8		
	OTU3e1			111.4		
	OTU3e2			111.5		

1.2V MDIO Interface Specifications

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Input Voltage	V_{IH}	0.84		1.5	V	
	V_{IL}	-0.3		0.36	V	
Input Leak current	I_{IN}	-100		100	uA	
Output Voltage	V_{OH}	1.0		1.5	V	
	V_{OL}	-0.3		0.2	V	
Input Capacitance	C_I			10	pF	
Input MDC Clock	f_{MDC}	0.1		4	MHz	
MDC Clock Period	T_{MDC}	250		10000	ns	
MDIO Hold Time	T_{hold}	10			ns	
MDIO SetupTime	T_{setup}	10			ns	
GLB_ALM	$T_{glb_alm_ass}$			150	ms	
	$T_{glb_alm_dea}$			150	ms	

Performance Specifications - Electrical

Parameter		Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter							
Input Amplitude (Differential)		Vin	150		1050	mVpp	AC coupled inputs*(Note6)
Input Impedance (Differential)		Zin	85	100	115	ohms	Rin > 100 kohms @ DC
TX_DIS	Disable	V_{IH}	2		Vcc+0.3	V	
	Enable	V_{IL}	0		0.8		
Receiver							
Output Amplitude (Differential)		Vout	340		850	mVpp	AC coupled outputs*(Note6)
Output Impedance (Differential)		Zout	85	100	115	ohms	
Output Rise/Fall Time		t_r/t_f	24			ps	20%~80%
RX_LOS	LOS	V_{OH}	2.4		Vcc+0.3	V	
	Normal	V_{OL}	0		0.8	V	

Optical and Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
9μm Core Diameter SMF	L			80	km
Transmitter					
Side Mode Suppression Ratio	SMSR	30			dB
Total Average Output Power*(Note4)	Po			13	dBm
Average Launch Power after AWG, per Lane	Peach	0		4	dBm
Extinction Ratio*(Note5)	ER	8.5			dB
Optical Modulation Amplitude (OMA), each lane		-4			dBm
Transmitter and dispersion penalty each lane	TDP			3	dB
Average launch power of OFF transmitter, each lane				-30	dBm
RIN				-120	dB/Hz
-20dB bandwidth， each lane				0.3	nm
Receiver					
Average Receive Power before AWG, per Lane	P_{IN}			-3	dBm
Average receive Sensitivity before AWG, each lane		-30			dBm
Damage threshold before AWG, each lane	P_{MAX}	0			dBm
Dispersion Tolerance, each lane		1600			Ps/nm

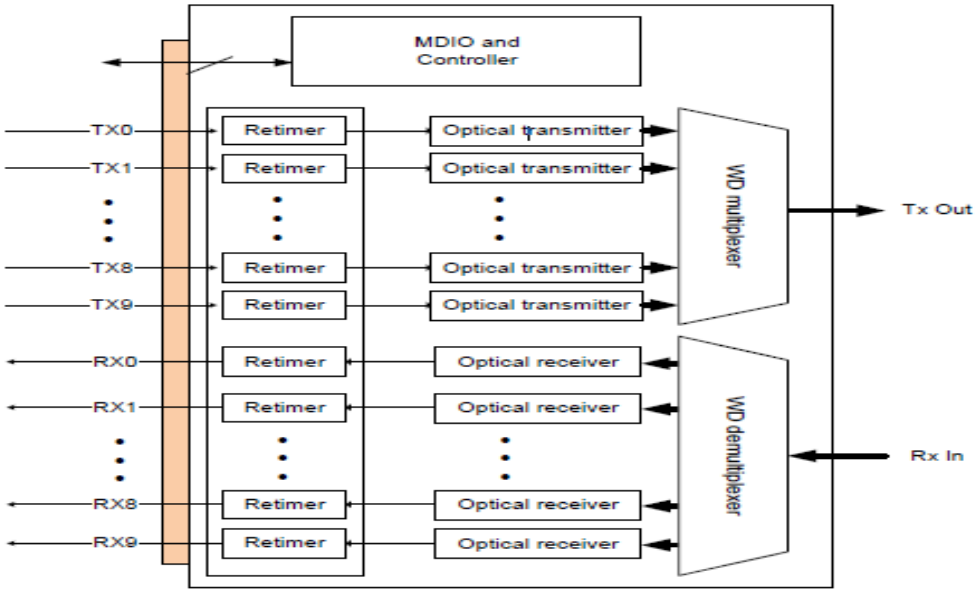
Receiver 3 dB electrical upper cutoff frequency, each lane		7.5			GHz
Receiver reflectance				-26	dB
Rx Loss assert total average input power level – typ +/-1dB			-25		dBm
Rx Loss Dassert total average input power level – typ +/-1dB			-24		dBm

Note4: Output is coupled into a 9/125μm single-mode fiber.

Note5: Filtered, measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps

Note6: High speed I/O, internally AC coupled.

Functional Description of Transceiver



REF Clock input

Required Clock frequency at Fb/64, Fb- CAUI data rate

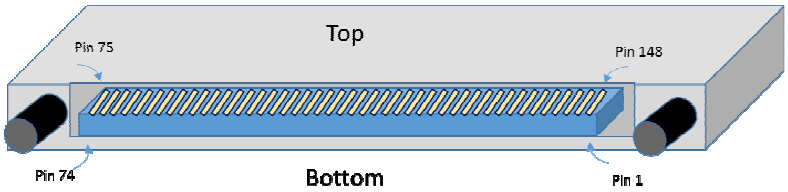
Rx Power Monitor implementation

Due to the use of EFDA on the Rx input, Rx power monitor per lane is not available.
However, the host can read the EDFA output power per lane on same MDIO Receiver Input Power monitor A/D registers A2D0, A2D1 (Units are in LSB=0.1Uw)
In additional, the host can read the total average input power on the Rx input port on MDIO register A032 (Units are in LSB=0.1Uw).

Rx LOS implementation

Rx LOS HW pin is generated from the total Rx input power monitor. This signal is also duplicated on all “Lane RX_LOS” bits in the MSA registers A210, A211, A212 (bit 4).

CFP Transceiver Electrical Pad Layout



Pin Function Definitions

CFP Top Row			
148	GND	111	GND
147	REFCLKn	110	N.C.
146	REFCLKp	109	N.C.
145	GND	108	GND
144	N.C.	107	RX9n
143	N.C.	106	RX9p
142	GND	105	GND
141	TX9n	104	RX8n
140	TX9p	103	RX8p
139	GND	102	GND
138	TX8n	101	RX7n
137	TX8p	100	RX7p
136	GND	99	GND
135	TX7n	98	RX6n
134	TX7p	97	RX6p
133	GND	96	GND
132	TX6n	95	RX5n
131	TX6p	94	RX5p
130	GND	93	GND
129	TX5n	92	RX4n
128	TX5p	91	RX4p
127	GND	90	GND
126	TX4n	89	RX3n
125	TX4p	88	RX3p
124	GND	87	GND
123	TX3n	86	RX2n
122	TX3p	85	RX2p
121	GND	84	GND
120	TX2n	83	RX1n
119	TX2p	82	RX1p
118	GND	81	GND

CFP Bottom Row			
1	3.3V_GND	38	MOD_ABS
2	3.3V_GND	39	MOD_RSTn
3	3.3V_GND	40	RX_LOS
4	3.3V_GND	41	GLB_ALRMn
5	3.3V_GND	42	PRTADR4
6	3.3V	43	PRTADR3
7	3.3V	44	PRTADR2
8	3.3V	45	PRTADR1
9	3.3V	46	PRTADR0
10	3.3V	47	MDIO
11	3.3V	48	MDC
12	3.3V	49	GND
13	3.3V	50	VND_IO_F
14	3.3V	51	VND_IO_G
15	3.3V	52	GND
16	3.3V_GND	53	VND_IO_H
17	3.3V_GND	54	VND_IO_J
18	3.3V_GND	55	3.3V_GND
19	3.3V_GND	56	3.3V_GND
20	3.3V_GND	57	3.3V_GND
21	VND_IO_A	58	3.3V_GND
22	VND_IO_B	59	3.3V_GND
23	GND	60	3.3V
24	*(TX_MCLKn)*	61	3.3V
25	*(TX_MCLKp)*	62	3.3V
26	GND	63	3.3V
27	VND_IO_C	64	3.3V
28	VND_IO_D	65	3.3V
29	VND_IO_E	66	3.3V
30	PRG_CNTL1	67	3.3V
31	PRG_CNTL2	68	3.3V

117	TX1n	80	RX0n
116	TX1p	79	RX0p
115	GND	78	GND
114	TX0n	77	(RX_MCLKn)
113	TX0p	76	(RX_MCLKp)
112	GND	75	GND

32	PRG_CNTL3	69	3.3V
33	PRG_ALRM1	70	3.3V_GND
34	PRG_ALRM2	71	3.3V_GND
35	PRG_ALRM3	72	3.3V_GND
36	TX_DIS	73	3.3V_GND
37	MOD_LOPWR	74	3.3V_GND

Bottom Row Pin Descriptions

Pin Num.	Name	Function	Notes
1	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
2	3.3V_GND		
3	3.3V_GND		
4	3.3V_GND		
5	3.3V_GND		
6	3.3V	3.3V Module Supply Voltage	3.3V ± 5%
7	3.3V		
8	3.3V		
9	3.3V		
10	3.3V		
11	3.3V		
12	3.3V		
13	3.3V		
14	3.3V		
15	3.3V		
16	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
17	3.3V_GND		
18	3.3V_GND		
19	3.3V_GND		
20	3.3V_GND		
21	VND_IO_A	I/O	Module Vendor I/O, NC
22	VND_IO_B	I/O	Module Vendor I/O, NC
23	GND	Ground	Signal Ground
24	*(TX_MCLKn)*	Tx Monitor Clock	Not Supported
25	*(TX_MCLKp)*	O	Not Connected Internally
26	GND	Ground	Signal Ground
27	VND_IO_C	I/O	Module Vendor I/O, NC
28	VND_IO_D	I/O	Module Vendor I/O, NC
29	VND_IO_E	I/O	Module Vendor I/O, NC
30	PRG_CNTL1	I	LVCOMS
31	PRG_CNTL2	I	LVCOMS
32	PRG_CNTL3	I	LVCOMS
33	PRG_ALRM1	O	LVCOMS
34	PRG_ALRM2	O	LVCOMS

35	PRG_ALRM3	O	LVCOMS
36	TX_DIS	Transmitter Disable I	“1” or NC = transmitter disabled, “0” = transmitter enabled
37	MOD_LOPWR	Module Low Power Mode I	“1” or NC: module in low power (safe) mode, “0”: power-on enabled
38	MOD_ABS	Module Absent O	“1” or NC: module absent, “0”: module present
39	MOD_RSTn	Module Reset I	“0” resets the module, “1” or NC = module enabled
40	RX_LOS	Loss of Signal O	“1”: low optical signal, “0”: normal condition
41	GLB_ALRMn	Global Alarm O	“0”: alarm condition in any MDIO Alarm register, “1”: no alarm condition
42	PRTADR4	1.2V CMOS I	MDIO Physical Port address bit4
43	PRTADR3	1.2V CMOS I	MDIO Physical Port address bit3
44	PRTADR2	1.2V CMOS I	MDIO Physical Port address bit2
45	PRTADR1	1.2V CMOS I	MDIO Physical Port address bit1
46	PRTADR0	1.2V CMOS I	MDIO Physical Port address bit0
47	MDIO	1.2V CMOS I/O	Management Data I/O bi-directional data
48	MDC	1.2V CMOS I	Management Data Clock
49	GND	Ground	Signal Ground
50	VND_IO_F	I/O	Module Vendor I/O, Not Connected Internally
51	VND_IO_G	I/O	Module Vendor I/O, Not Connected Internally
52	GND	Ground	Signal Ground
53	VND_IO_H	I/O	Module Vendor I/O, Not Connected Internally
54	VND_IO_J	I/O	Module Vendor I/O, Not Connected Internally
55	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
56	3.3V_GND		
57	3.3V_GND		
58	3.3V_GND		
59	3.3V_GND		

60	3.3V	3.3V Module Supply Voltage	3.3V ± 5%
61	3.3V		
62	3.3V		
63	3.3V		
64	3.3V		
65	3.3V		
66	3.3V		
67	3.3V		
68	3.3V		
69	3.3V		
70	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
71	3.3V_GND		
72	3.3V_GND		
73	3.3V_GND		
74	3.3V_GND		

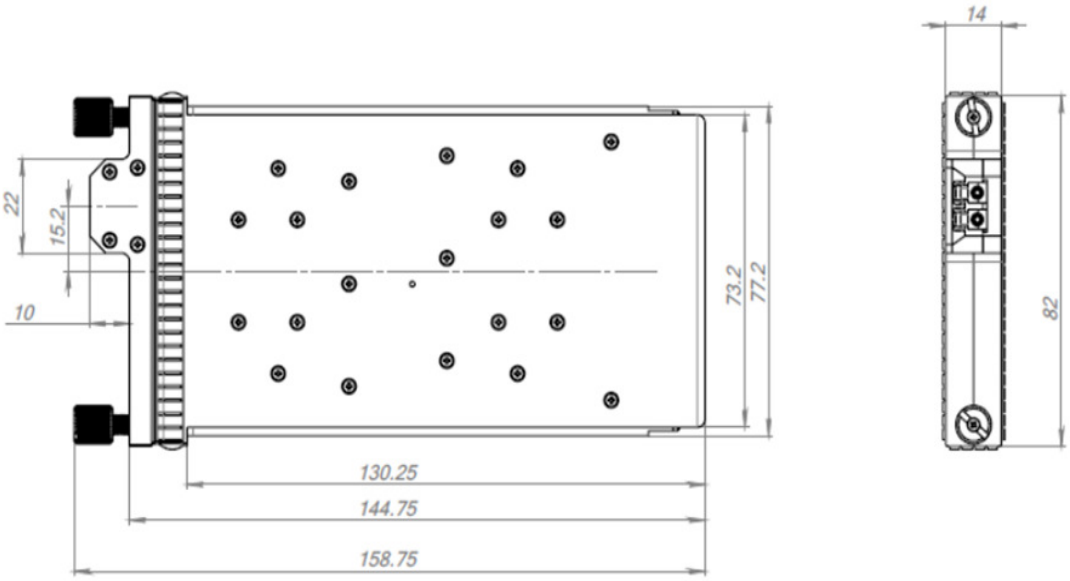
Top Row Pin Descriptions

Pin Num.	Name	Function	Notes
148	GND	Ground	Signal Ground
147	REFCLKn	Reference Clock I	Not Required
146	REFCLKp		Not Connected Internally
145	GND	Ground	Signal Ground
144	N.C.		Not Connected Internally
143	N.C.		Not Connected Internally
142	GND	Ground	Signal Ground
141	TX9n	Lane 9 Tx Input I	CML Input
140	TX9p		
139	GND	Ground	Signal Ground
138	TX8n	Lane 8 Tx Input I	CML Input
137	TX8p		
136	GND	Ground	Signal Ground
135	TX7n	Lane 7 Tx Input I	CML Input
134	TX7p		
133	GND	Ground	Signal Ground
132	TX6n	Lane 6 Tx Input I	CML Input
131	TX6p		
130	GND	Ground	Signal Ground
129	TX5n	Lane 5 Tx Input I	CML Input
128	TX5p		
127	GND	Ground	Signal Ground
126	TX4n	Lane 4 Tx Input I	CML Input
125	TX4p		
124	GND	Ground	Signal Ground
123	TX3n	Lane 3 Tx Input	CML Input

122	TX3p	I	
121	GND	Ground	Signal Ground
120	TX2n	Lane 2 Tx Input	CML Input
119	TX2p	I	
118	GND	Ground	Signal Ground
117	TX1n	Lane 1 Tx Input	CML Input
116	TX1p	I	
115	GND	Ground	Signal Ground
114	TX0n	Lane 0 Tx Input	CML Input
113	TX0p	I	
112	GND	Ground	Signal Ground
111	GND	Ground	Signal Ground
110	N.C.		Not Connected Internally
109	N.C.		Not Connected Internally
108	GND	Ground	Signal Ground
107	RX9n	Lane 9 Rx Output	CML Output
106	RX9p	O	
105	GND	Ground	Signal Ground
104	RX8n	Lane 8 Rx Output	CML Output
103	RX8p	O	
102	GND	Ground	Signal Ground
101	RX7n	Lane 7 Rx Output	CML Output
100	RX7p	O	
99	GND	Ground	Signal Ground
98	RX6n	Lane 6 Rx Output	CML Output
97	RX6p	O	
96	GND	Ground	Signal Ground
95	RX5n	Lane 5 Rx Output	CML Output
94	RX5p	O	
93	GND	Ground	Signal Ground
92	RX4n	Lane 4 Rx Output	CML Output
91	RX4p	O	
90	GND	Ground	Signal Ground
89	RX3n	Lane 3 Rx Output	CML Output
88	RX3p	O	
87	GND	Ground	Signal Ground
86	RX2n	Lane 2 Rx Output	CML Output
85	RX2p	O	
84	GND	Ground	Signal Ground
83	RX1n	Lane 1 Rx Output	CML Output
82	RX1p	O	
81	GND	Ground	Signal Ground
80	RX0n	Lane 0 Rx Output	CML Output
79	RX0p	O	

78	GND	Ground	Signal Ground
77	*(RX_MCLKn)*	Rx Monitor Clock	Not Supported
76	*(RX_MCLKp)*	O	Not Connected Internally
75	GND	Ground	Signal Ground

Mechanical Specifications



*This 2D drawing only for reference, please check with Eoptolink before ordering.

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Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Abby	Kelly		Preliminary initial.	April 23, 2013
V1.b	Abby	Kelly		Update Mechanical Specification	May 7, 2014
V1.c	Angela	Kelly		Add product picture.	May 8,2014
V1.d	Abby	Kelly		Update some parameters	Jan 26,, 2015
V1.e	Angela	Jason		Update the Total Average Output Power (from 8dB to 13dB) and Optical Modulation Amplitude (OMA), each lane (from -7~-2dB to 0~4dB).	Feb 16,2015
V1.f	Abby	Kelly		Update Mechanical Specification	Jun 15, 2015

V1.g	Angela	Kelly/ Jason		Update the product picture, 2d drawing and regulatory compliance.	Mar 18,2016

Notice:

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