

# EOLC-161HG-C-20-L1A Series

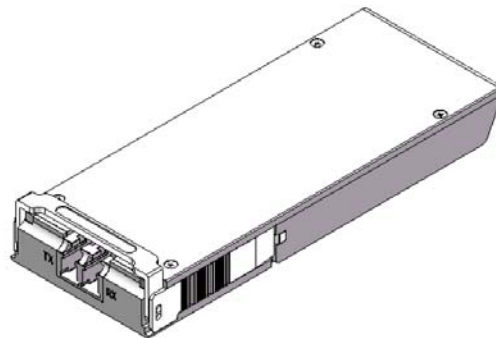
Single-Mode OTU4 4I1-9D1F CFP2 Transceiver

Single-Mode 100GBASE-LR4 CFP2 Transceiver

RoHS6 Compliant

## Features

- ◆ Supports 103Gbps and 112Gbps aggregate bit rates
- ◆ Single 3.3V Power Supply and Power dissipation < 6W
- ◆ Up to 20km transmission on SMF
- ◆ Hot-Pluggable CFP2 Footprint Duplex LC Connector Interface
- ◆ Class 1 FDA and IEC60825-1 Laser Safety Compliant
- ◆ RoHS6 Compliant
- ◆ Operating Case Temperature Standard: 0°C~+70°C
- ◆ Compliant with CFP2 MSA Specification
- ◆ MDIO interface with integrated Digital Diagnostic Monitoring
- ◆ 4 x 28G electrical interface



## Applications

- ◆ 100GBASE-LR4 Ethernet
- ◆ OTU4 4I1-9D1F

## Ordering Information

Part No.	Data Rate <sup>*not e2</sup>	Fiber	Distance <sup>*note1</sup>	Interface	Temp.	DDMI
EOLC-161HG-C-20-L1A	112Gbps	SMF	20km	LC	Standard	Yes

Note1: 20 km with 9/125µm SMF

Note2: Switching between 100GBASE-LR4 and OTU4 4I1-9D1F through MDIO.

\*The product image only for reference purpose.

## Regulatory Compliance\*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

\*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FCC, FDA and ROHS. For the latest certification information, please check with Eoptolink.

## Absolute Maximum Ratings<sup>\*note3</sup>

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%
ESD <sup>*note4</sup>			500	V

Note3: Exceeding any one of these values may destroy the device immediately.

Note4: Human body model.

## Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T <sub>C</sub> EOLC-161HG-C-20-L1A	0		+70	°C
Power Supply Voltage	Vcc	3.2	3.3	3.4	V
Power Consumption	P			9	W

## Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
<b>Transmitter</b>						
Input Amplitude (Differential)	V <sub>in</sub>			900	mVpp	AC coupled inputs <sup>*(Note7)</sup>
Input Impedance (Differential)	Z <sub>in</sub>	85	100	115	ohms	R <sub>in</sub> > 100 kohms @ DC
<b>Receiver</b>						
Output Amplitude (Differential)	V <sub>out</sub>			900	mVpp	AC coupled outputs <sup>*(Note7)</sup>
Output Impedance (Differential)	Z <sub>out</sub>	85	100	115	ohms	

### 1.2V MDIO Interface Specifications

Parameter	Symbol	Min.	Max	Unit
Input Voltage	$V_{IH}$	0.84	1.5	V
	$V_{IL}$	-0.3	0.36	V
Input Leak current	$I_{IN}$	-100	100	uA
Output Voltage	$V_{OH}$	1.0	1.5	V
	$V_{OL}$	-0.3	0.2	V
Input Capacitance	$C_I$		10	pF
Input MDC Clock	$f_{MDC}$	0.1	4	MHz
MDC Clock Period	$T_{MDC}$	250	10000	ns
MDIO Hold Time	$T_{hold}$	10		ns
MDIO SetupTime	$T_{setup}$	10		ns
Clock to output delay from the MMD	$T_{dely}$	0	300	ns
GLB_ALM	$T_{glb\_alm\_ass}$		150	ms
	$T_{glb\_alm\_dea}$		150	ms
MDC High time	$T_{high}$		160	ns
MDC Low time	$T_{low}$		160	ns

### Optical and Electrical Characteristics

#### OTU4 4I1-9D1F Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Transmitter</b>					
Signaling Speed per Lane	$BR_{AVE}$		27.95		Gbps
Data Rate Variation		-20		+20	ppm
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm
Total Average Output Power <sup>*(Note5, Note6)</sup>	$P_{O1}$	-		8.9	dBm
Average Launch Power per Lane <sup>*(Note6)</sup>	$P_{each1}$	-2.5		2.9	dBm
Maximum channel power difference				5	dB
Channel spacing			800		GHz
Maximum spectral excursion		-184		184	GHz
Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Extinction Ratio <sup>*(Note6)</sup>	$ER_1$	7			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} <sup>*(Note6)</sup>		G.959.1 Compliant			
TX Disable Assert Time	$t_{off}$			100	us
<b>Receiver</b>					

Signaling Speed per Lane	$BR_{AVE}$		27.95		Gbps
Data Rate Variation		-20		+20	ppm
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane <sup>*(Note9)</sup>	$R_{pow1}$	-9.5		4	dBm
Equivalent Sensitivity per Lane <sup>*(Note11)</sup>	$P_{min1}$			-11	dBm
Damage Threshold per Lane	$P_{max}$	5.5			dBm
Maximum channel power difference				5.5	dB
Maximum optical path penalty				1.5	dB
Optical Return Loss	ORL			-26	dB
LOS Assert	LOSA	-21	-17	-16	dBm
LOS De-Assert	LOSD		-16	-15	dBm
LOS Hysteresis		0.5			dB

### 100GBASE-LR4 Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Transmitter</b>					
Signaling Speed per Lane	$BR_{AVE}$		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm
Total Average Output Power <sup>*(Note5, Note8)</sup>	$P_{O2}$	-		10.5	dBm
Average Launch Power per Lane <sup>*(Note8)</sup>	$P_{each2}$	-4.3		4.5	dBm
Side Mode Suppression Ratio	SMSR	30			dB
Difference in launch power between any two lanes				5	dB
Average launch power of OFF transmitter per lane				-30	dBm
Optical Return Loss Tolerance				20	dB
Transmitter reflectance				-12	dB
Extinction Ratio <sup>*(Note8)</sup>	ER	4			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} <sup>*(Note8)</sup>		IEEE802.3ba-2010 Compliant			
TX Disable Assert Time	$t_{off}$			100	us
<b>Receiver</b>					
Signaling Speed per Lane	$BR_{AVE}$		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	$\lambda_{C0}$	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	$\lambda_{C1}$	1299.02	1300.05	1301.09	nm

Lane_2 Center Wavelength	$\lambda_{C2}$	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	$\lambda_{C3}$	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane*(Note10)	$R_{pow2}$	-10.6		4.5	dBm
Receive Sensitivity(OmA) per Lane*(Note12)	$P_{min2}$			-9.8	dBm
Stressed Sensitivity(OmA) per lane	SRS			-6.8	dBm
Damage Threshold per Lane	$P_{max}$	5.5			dBm
Optical Return Loss	ORL			-26	dB
LOS Assert	LOSA	-21	-17	-16	dBm
LOS De-Assert	LOSD		-16	-15	dBm
LOS Hysteresis*(Note13)		0.5			dB

Note5: Output is coupled into a 9/125 $\mu$ m single-mode fiber.

Note6: Filtered, measured with a PRBS 2<sup>31</sup>-1 test pattern @27.95Gbps

Note7: High speed I/O, internally AC coupled.

Note8: Filtered, measured with a PRBS 2<sup>31</sup>-1 test pattern @25.78Gbps

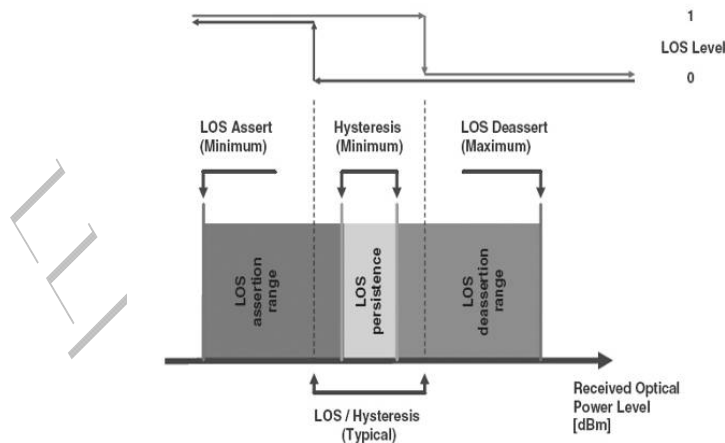
Note9: CFP2 transceiver works in OTU4 4I1-9D1F mode.

Note10: CFP2 transceiver works in 100GBASE-LR4 mode.

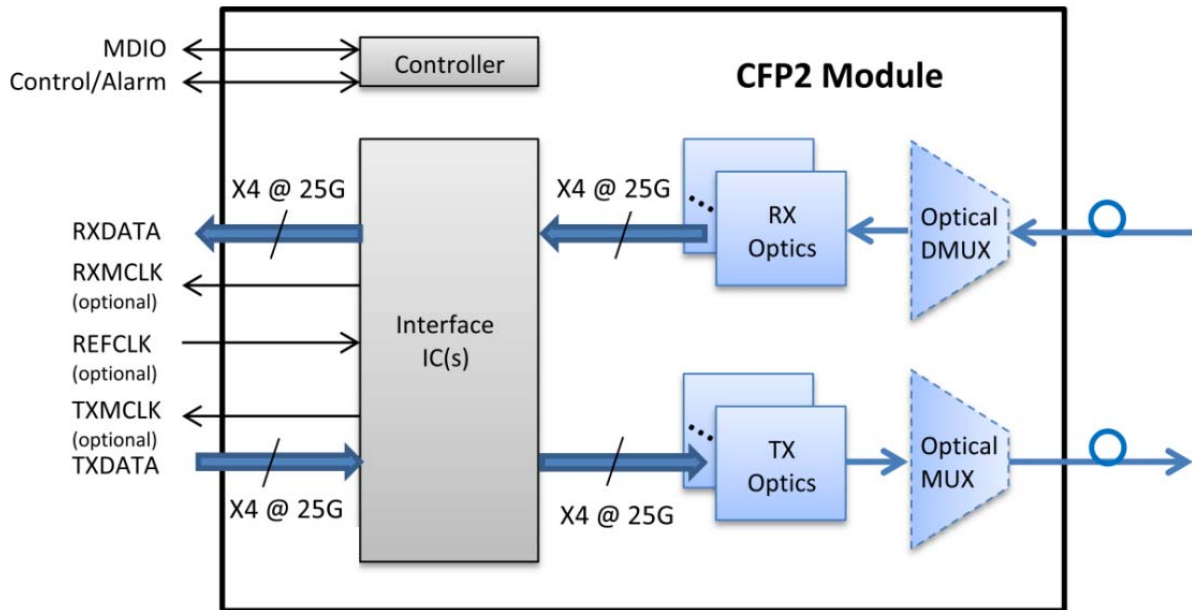
Note11: Minimum average optical power measured at BER less than 1E-12, with a 2<sup>31</sup>-1 PRBS@27.95Gbps.

Note12: Minimum average optical power measured at BER less than 1E-12, with a 2<sup>31</sup>-1 PRBS@25.78Gbps.

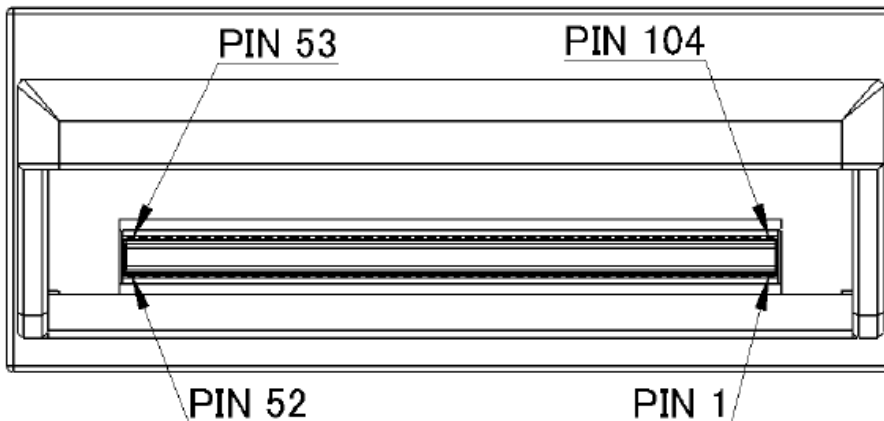
Note13: LOS Hysteresis



### Functional Description of Transceiver



### CFP2 Transceiver Electrical Pad Layout



### Pin Function Definitions

CFP2 Bottom	
1	GND
2	(TX_MCK_N)
3	(TX_MCK_P)
4	GND
5	N.C.
6	N.C.
7	3.3V_GND
8	3.3V_GND
9	3.3V

CFP2 Top	
104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p

10	3.3V	95	GND
11	3.3V	94	N.C.
12	3.3V	93	N.C.
13	3.3V_GND	92	GND
14	3.3V_GND	91	N.C.
15	VND_IO_A	90	N.C.
16	VND_IO_B	89	GND
17	PRG_CNTL1	88	TX1n
18	PRG_CNTL2	87	TX1p
19	PRG_CNTL3	86	GND
20	PRG_ALARM1	85	TX0n
21	PRG_ALARM2	84	TX0p
22	PRG_ALARM3	83	GND
23	GND	82	N.C.
24	TX_DIS	81	N.C.
25	RX_LOS	80	GND
26	MOD_LOPWR	79	(REFCLKn)
27	MOD_ABS	78	(REFCLKp)
28	MOD_RSTn	77	GND
29	GLB_ALRMn	76	N.C.
30	GND	75	N.C.
31	MDC	74	GND
32	MDIO	73	RX3n
33	PRTADR0	72	RX3p
34	PRTADR1	71	GND
35	PRTADR2	70	RX2n
36	VND_IO_C	69	RX2p
37	VND_IO_D	68	GND
38	VND_IO_E	67	N.C.
39	3.3V_GND	66	N.C.
40	3.3V_GND	65	GND
41	3.3V	64	N.C.
42	3.3V	63	N.C.
43	3.3V	62	GND
44	3.3V	61	RX1n
45	3.3V_GND	60	RX1p
46	3.3V_GND	59	GND
47	N.C.	58	RX0n
48	N.C.	57	RX0p
49	GND	56	GND
50	(RX_MCK_N)	55	N.C.
51	(RX_MCK_P)	54	N.C.
52	GND	53	GND

## Bottom Row Pin Descriptions

Pin Num.	Name	Function	Notes
1	GND		
2	(TX_MCK_N)	O CML	For optical waveform testing. Not for normal use.
3	(TX_MCK_P)	O CML	For optical waveform testing. Not for normal use.
4	GND		
5	N.C.		
6	N.C.		
7	3.3V_GND		3.3V Module Supply Voltage
8	3.3V_GND		
9	3.3V		
10	3.3V		
11	3.3V		
12	3.3V		
13	3.3V_GND		
14	3.3V_GND		
15	VND_IO_A		Module Vendor I/O A. Do not connect!
16	VND_IO_B		Module Vendor I/O B. Do not connect!
17	PRG_CNTL1		Programmable control 1 set over MDIO, MSA default: TRXIC_RSTn. TX&RX ICs reset. "0": reset; "1" or NC: enabled = not used.
18	PRG_CNTL2		Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used
19	PRG_CNTL3		Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used
20	PRG_ALARM1		Programmable alarm 1 set over MDIO, MSA default: HIPWR_ON. "1": module power up completed; "0": module not high powered up.
21	PRG_ALARM2		Programmable alarm 2 set over MDIO, MSA default: MOD_READY. "1": ready; "0": not ready.
22	PRG_ALARM3		Programmable alarm 3 set over MDIO, MSA default: MOD_FAULT, fault detected. "1": fault; "0": not fault.
23	GND		
24	TX_DIS	I LVCMOS	Transmitter disable for all lanes. "1" or NC: transmitter disabled; "0": transmitter enabled.
25	RX_LOS	O LVCMOS	Receiver loss of optical signal. "1": low optical signal; "0": normal condition.
26	MOD_LOPWR	I LVCMOS	Module Low power mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled.



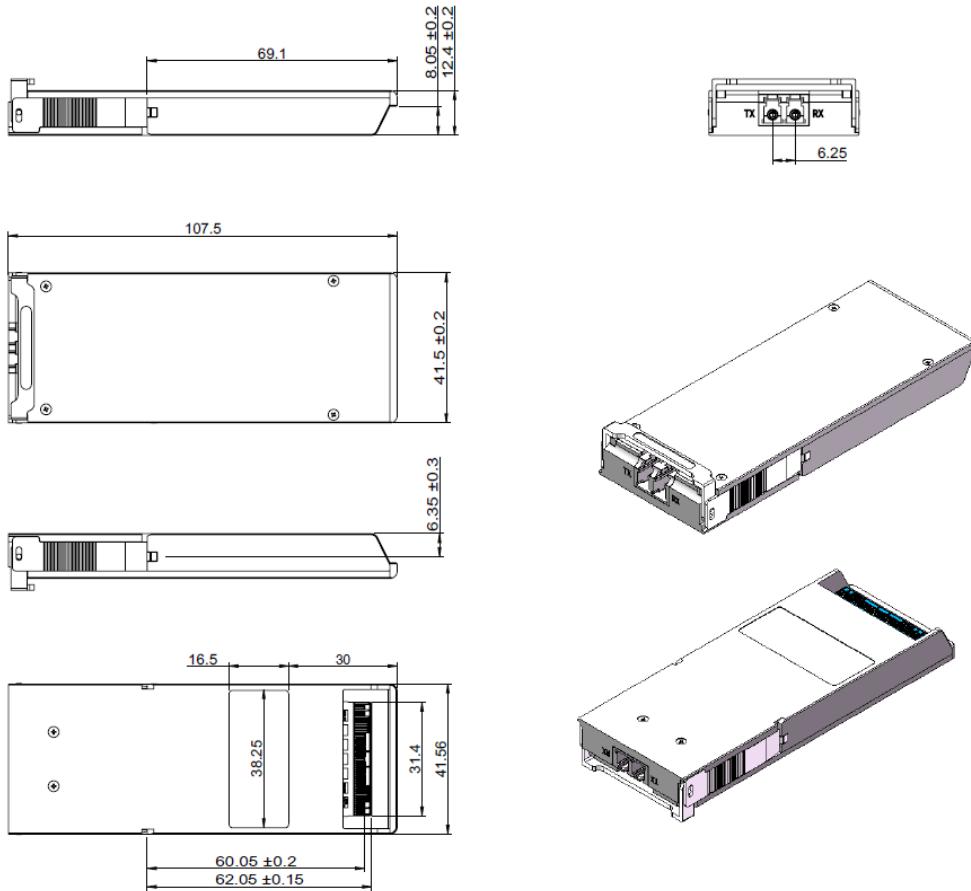
27	MOD_ABS	O GND	Module Absent. "1" or NC: module absent; "0": module present. Pull up resistor on Host.
28	MOD_RSTn	I LVCMOS	Module Reset. "0": resets the module; "1" or NC: module enabled. Pull Down Resistor in module.
29	GLB_ALRMn	O LVCMOS	Global Alarm. "0": alarm condition in any MDIO alarm register; "1": no alarm condition. Open Drain, Pull up resistor on Host
30	GND		
31	MDC	I 1.2V CMOS	Management Data Clock
32	MDIO	I/O 1.2V CMOS	Management Data I/O bi-directional data
33	PRTADR0	I 1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I 1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I 1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O	Module Vendor I/O C. Do not connect!
37	VND_IO_D	I/O	Module Vendor I/O D. Do not connect!
38	VND_IO_E	I/O	Module Vendor I/O E. Do not connect!
39	3.3V_GND		
40	3.3V_GND		
41	3.3V		3.3V Module Supply Voltage
42	3.3V		
43	3.3V		
44	3.3V		
45	3.3V_GND		
46	3.3V_GND		
47	N.C.		No Connect
48	N.C.		No Connect
49	GND		
50	(RX_MCK_N)	O CML	For optical waveform testing. Not for normal use.
51	(RX_MCK_P)	O CML	For optical waveform testing. Not for normal use.
52	GND		

### Top Row Pin Descriptions

Pin Num.	Name	Function	Notes
53	GND		
54	N.C.		
55	N.C.		
56	GND		
57	RX0p	Lane 0 Rx Output	CML Output
58	RX0n	O	
59	GND		
60	RX1p	Lane 1 Rx Output	CML Output
61	RX1n	O	
62	GND		

63	N.C.		
64	N.C.		
65	GND		
66	N.C.		
67	N.C.		
68	GND		
69	RX2p	Lane 2 Rx Output	CML Output
70	RX2n	O	
71	GND		
72	RX3p	Lane 3 Rx Output	CML Output
73	RX3n	O	
74	GND		
75	N.C.		
76	N.C.		
77	GND		
78	(REFCLKn)	Reference Clock	Reference Clock Input
79	(REFCLKp)	I	
80	GND		
81	N.C.		
82	N.C.		
83	GND		
84	TX0p	Lane 0 Tx Input	CML Input
85	TX0n	I	
86	GND		
87	TX1p	Lane 1 Tx Input	CML Input
88	TX1n	I	
89	GND		
90	N.C.		
91	N.C.		
92	GND		
93	N.C.		
94	N.C.		
95	GND		
96	TX2p	Lane 2 Tx Input	CML Input
97	TX2n	I	
98	GND		
99	TX3p	Lane 3 Tx Input	CML Input
100	TX3n	I	
101	GND		
102	N.C.		
103	N.C.		
104	GND		

## Mechanical Specifications



## CFP2

\*This 2D drawing only for reference, please check with Eoptolink before ordering.

## Obtaining Document

You can visit our website: <http://www.eoptolink.com>

Or contact Eoptolink Technology Inc., Ltd. listed at the end of the documentation to get the latest documents.

## Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Arvin/Quintus	Phlio/Jason		New released.	Jun 25, 2017

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