

EOLC-851HG-02-MOYO Series

**Multi-Mode 100GBASE-SR10
CFP Transceiver
RoHS6 Compliant**



Features

- ◆ Compliant to the IEEE 802.3ba(100GBASE-SR10)
- ◆ Support interoperability with IEEE 802.3ae 10GBASE-SR modules of various form factors such as SFP+, XFP, X2
- ◆ Compliant to the CFP MSA Specification
- ◆ Up to 100m on OM3 and 150m on OM4 MMF
- ◆ VCSEL array transmitter and PIN array receiver
- ◆ Single 3.3V Power Supply and Power dissipation $\leq 8W$
- ◆ Operates at 10.3125Gbps per channel
- ◆ 111.809Gbit/s for OTU4 compatible
- ◆ Operating Case Temperature: 0°C~+70°C
- ◆ MDIO digital diagnostic interface and control capabilities
- ◆ Utilizes a standard 24/20 lane optical fiber with MPO connector

Applications

- ◆ 100GBE and 10GBE interconnects
- ◆ Datacom/Telecom switch & router connections
- ◆ Data aggregation and backplane applications
- ◆ Proprietary protocol and density application

Ordering Information

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
EOLC-851HG-02-MOYO *(note1)	112Gbps	MMF	100m/150m	MPO	0°C ~+70°C	Yes

Note1: Standard version

Note2: 100m with OM3 MMF and 150m with OM4 MMF

Regulatory Compliance*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Eoptolink.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T _s	-40	+85	°C
Supply Voltage	V _{cc}	-0.5	3.6	V
Operating Relative Humidity(non-condensing)	RH	5	85	%

*Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T _C EOLC-851HG-02-MOYO	0	-	+70	°C
Power Supply Voltage	V _{cc}	3.2	3.3	3.4	V
Power Dissipation	P _m	-	-	8	W
Low Power Mode Dissipation	P _{low}	-	-	2	w
Aggregate Bit Rate	BR _{Aggr}	-	103.125	111.809	Gbps
Lane Bit Rate	BR _{LANE}	-	10.3125	11.1809	Gbps

Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
AC common mode input voltage tolerance		-	-	20	mV	RMS
Input Impedance (Differential)	Z _{in}	90	100	110	ohms	

Input High Voltage	V_{IH}	2	-	$V_{CC}+0.3$	V	3.3V LVCMOS
		0.84	-	1.5	V	1.2V LVCMOS
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	3.3V LVCMOS
		-0.3	-	0.36	V	1.2V LVCMOS
Receiver						
Differential output voltage, peak-to-peak		-	-	760	mV	
AC common mode output voltage		-	-	15	mV	RMS
Termination mismatch at 1MHz		-	-	5	%	
Output impedance (Differential)	Z_{out}	90	100	110	ohms	
Output rise and fall time		24			ps	20%~80%
Output High Voltage	V_{OH}	$V_{CC}-0.2$	-	-	V	3.3V LVCMOS ($I_{OH}=-100\mu A$)
		1.0	-	1.5	V	1.2V LVCMOS
Output Low Voltage	V_{OL}	-	-	0.2	V	3.3V LVCMOS ($I_{OL}=100\mu A$)
		-0.3	-	0.2	V	1.2V LVCMOS

Optical and Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
OM3 MMF	L	0.5	-	100	m
Aggregate Bit Rate	BR_{Aggr}	-	103.125	111.809	Gbps
Per Lane Bit Rate	BR_{LANE}	-	10.3125	11.1809	Gbps
Transmitter					
Center Wavelength	λ_C	840	850	860	nm
RMS spectral width	RMS	-	-	0.65	nm
Average Launch Power, Each Lane ^{*(note3)}	$P_{out}/lane$	-7.6	-	2.4	dBm
Transmit OMA, per Lane	$TX_OMA/lane$	-5.6	-	3	dBm
Difference in launch power between any two lanes(OMA)		-	-	4	dB
Peak power, each lane		-	-	4	dBm
Transmitter and dispersion penalty, each lane	TDP/lane	-	-	3.5	dB
Extinction Ratio ^{*(note4)}	ER	3	-	-	dB
Optical Return Loss Tolerance		-	-	12	dB
Average launch power of OFF		-	-	-30	dBm

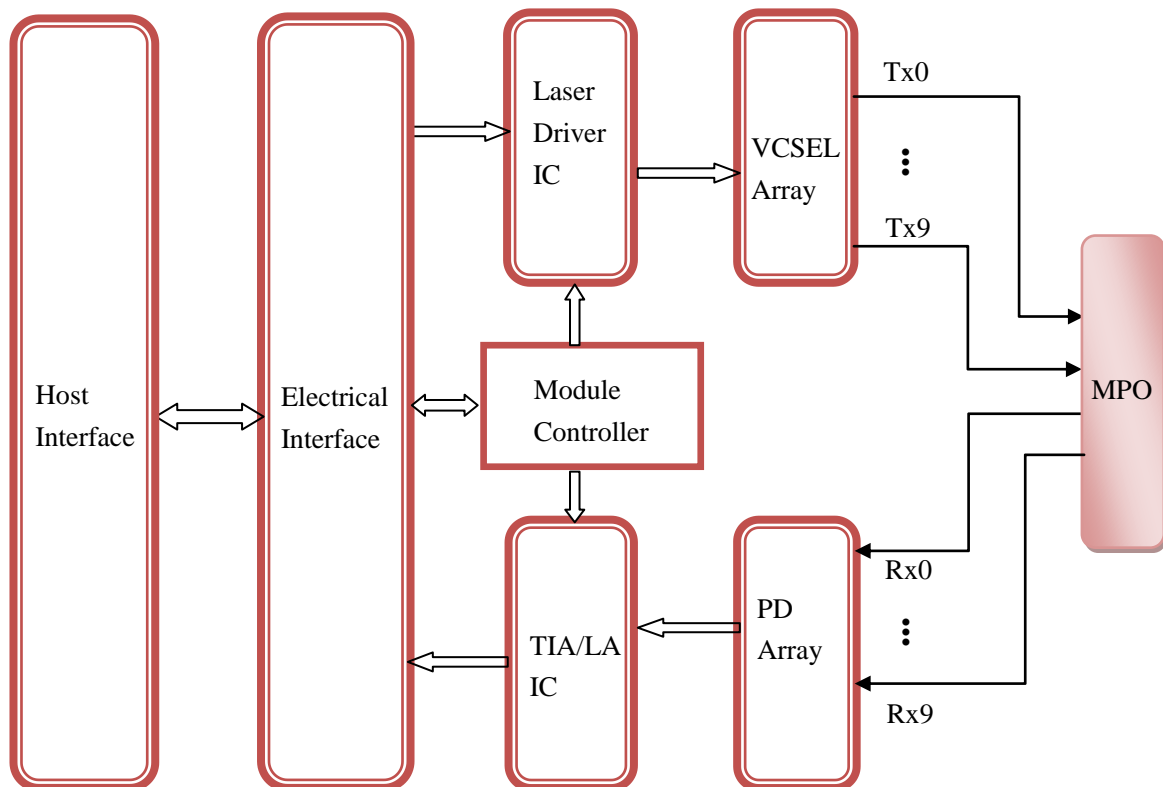
transmitter, each lane					
Output Optical Eye ^{*(note4)}	IEEE 802.3ba-2010 Compliant				
Receiver					
Center Wavelength	λ_c	840	850	860	nm
Damage Threshold		3.4	-	-	dBm
Optical modulation amplitude, each lane		-	-	3	dBm
Stressed receiver sensitivity in OMA, each lane		-	-	-5.4	dBm
Average power at receiver input, each lane	RX/lane	-9.5 ^{*(note5)}	-	+2.4	dBm
Peak power, each lane		-	-	4	dBm
Receiver reflectance	Rr	-	-	-12	dB

Note3: Output is coupled into a 50/125 μ m multi-mode fiber.

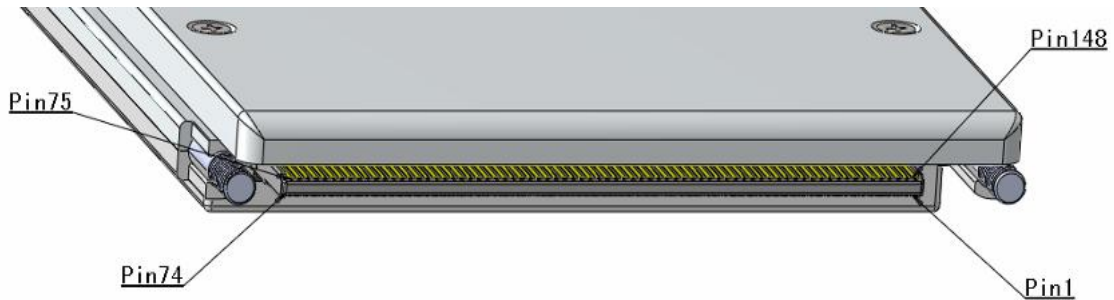
Note4: Filtered, measured with a PRBS 2³¹-1 test pattern @10.3125Gbps

Note5: Minimum average optical power measured at BER less than 1E-12, with a 2³¹-1 PRBS.

Functional Description of Transceiver



CFP Transceiver Electrical Pad Layout



	Top Row (2nd Half)		Bottom Row (2nd Half)		Top Row (1st Half)		Bottom Row (1st Half)
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	N.C.	39	MOD_RSTn
146	REFCLKp	3	3.3V_GND	109	N.C.	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	N.C.	5	3.3V_GND	107	RX9n	42	PRTADR4
143	N.C.	6	3.3V	106	RX9p	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	TX9n	8	3.3V	104	RX8n	45	PRTADR1
140	TX9p	9	3.3V	103	RX8p	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	TX8n	11	3.3V	101	RX7n	48	MDC
137	TX8p	12	3.3V	100	RX7p	49	GND
136	GND	13	3.3V	99	GND	50	VND_IO_F
135	TX7n	14	3.3V	98	RX6n	51	VND_IO_G
134	TX7p	15	3.3V	97	RX6p	52	GND
133	GND	16	3.3V_GND	96	GND	53	VND_IO_H
132	TX6n	17	3.3V_GND	95	RX5n	54	VND_IO_J
131	TX6p	18	3.3V_GND	94	RX5p	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	TX5n	20	3.3V_GND	92	RX4n	57	3.3V_GND
128	TX5p	21	VND_IO_A	91	RX4p	58	3.3V_GND
127	GND	22	VND_IO_B	90	GND	59	3.3V_GND
126	TX4n	23	GND	89	RX3n	60	3.3V
125	TX4p	24	(TX_MCLKn)	88	RX3p	61	3.3V
124	GND	25	(TX_MCLKp)	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	VND_IO_C	85	RX2p	64	3.3V
121	GND	28	VND_IO_D	84	GND	65	3.3V
120	TX2n	29	VND_IO_E	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	(RX_MCLKn)	72	3.3V_GND
113	TX0p	36	TX_DIS	76	(RX_MCLKp)	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

Pin Arrangement and Definition

Pin	Logic	Symbol	Description
1		3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2		3.3V_GND	

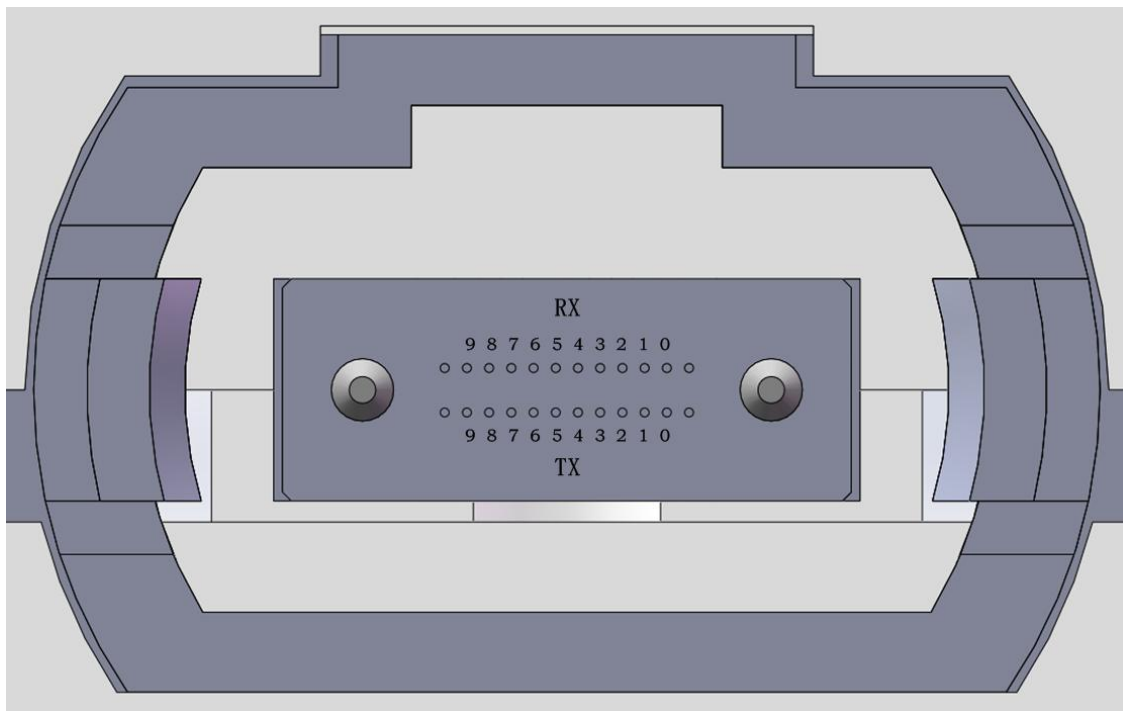
3		3.3V_GND	
4		3.3V_GND	
5		3.3V_GND	
6		3.3V	3.3V Module Supply Voltage
7		3.3V	
8		3.3V	
9		3.3V	
10		3.3V	
11		3.3V	
12		3.3V	
13		3.3V	
14		3.3V	
15		3.3V	
16		3.3V_GND	
17		3.3V_GND	
18		3.3V_GND	
19		3.3V_GND	
20		3.3V_GND	
21		VND_IO_A	Module Vendor I/O A. Do Not Connect!
22		VND_IO_B	Module Vendor I/O B. Do Not Connect!
23		GND	
24	CML	(TX_MCLKn)	For optical waveform testing. Not for normal use.
25	CML	(TX_MCLKp)	For optical waveform testing. Not for normal use.
26		GND	
27		VND_IO_C	Module Vendor I/O C. Do Not Connect!
28		VND_IO_D	Module Vendor I/O D. Do Not Connect!
29		VND_IO_E	Module Vendor I/O E. Do Not Connect!
30	LVC MOSw/PUR	PRG_CNTL1	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	LVC MOSw/PUR	PRG_CNTL2	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
32	LVC MOSw/PUR	PRG_CNTL3	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
33	LVC MOS	PRG_ALRM1	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high power up
34	LVC MOS	PRG_ALRM2	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready
35	LVC MOS	PRG_ALRM3	Programmable Alarm 3 set over MDIO, MSA Default:

CFP Series *Preliminary*

			MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	LVC MOSw/PUR	TX_DIS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	LVC MOSw/PUR	MOD_LOPWR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
38	GND	MOD_ABS	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	LVC MOSw/PDR	MOD_RSTn	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	LVC MOS	RX_LOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	LVC MOS	GLB_ALRMn	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	1.2V CMOS	PRTADR4	MDIO Physical Port address bit 4
43	1.2V CMOS	PRTADR3	MDIO Physical Port address bit 3
44	1.2V CMOS	PRTADR2	MDIO Physical Port address bit 2
45	1.2V CMOS	PRTADR1	MDIO Physical Port address bit 1
46	1.2V CMOS	PRTADR0	MDIO Physical Port address bit 0
47	1.2V CMOS	MDIO	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	1.2V CMOS	MDC	Management Data Clock (electrical specs as per 802.3ae and ba)
49		GND	
50		VND_IO_F	Module Vendor I/O F. Do Not Connect!
51		VND_IO_G	Module Vendor I/O G. Do Not Connect!
52		GND	
53		VND_IO_H	Module Vendor I/O H. Do Not Connect!
54		VND_IO_J	Module Vendor I/O J. Do Not Connect!
55		3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56		3.3V_GND	
57		3.3V_GND	
58		3.3V_GND	
59		3.3V_GND	
60		3.3V	3.3V Module Supply Voltage
61		3.3V	
62		3.3V	
63		3.3V	
64		3.3V	
65		3.3V	
66		3.3V	

67		3.3V	
68		3.3V	
69		3.3V	
70		3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71		3.3V_GND	
72		3.3V_GND	
73		3.3V_GND	
74		3.3V_GND	

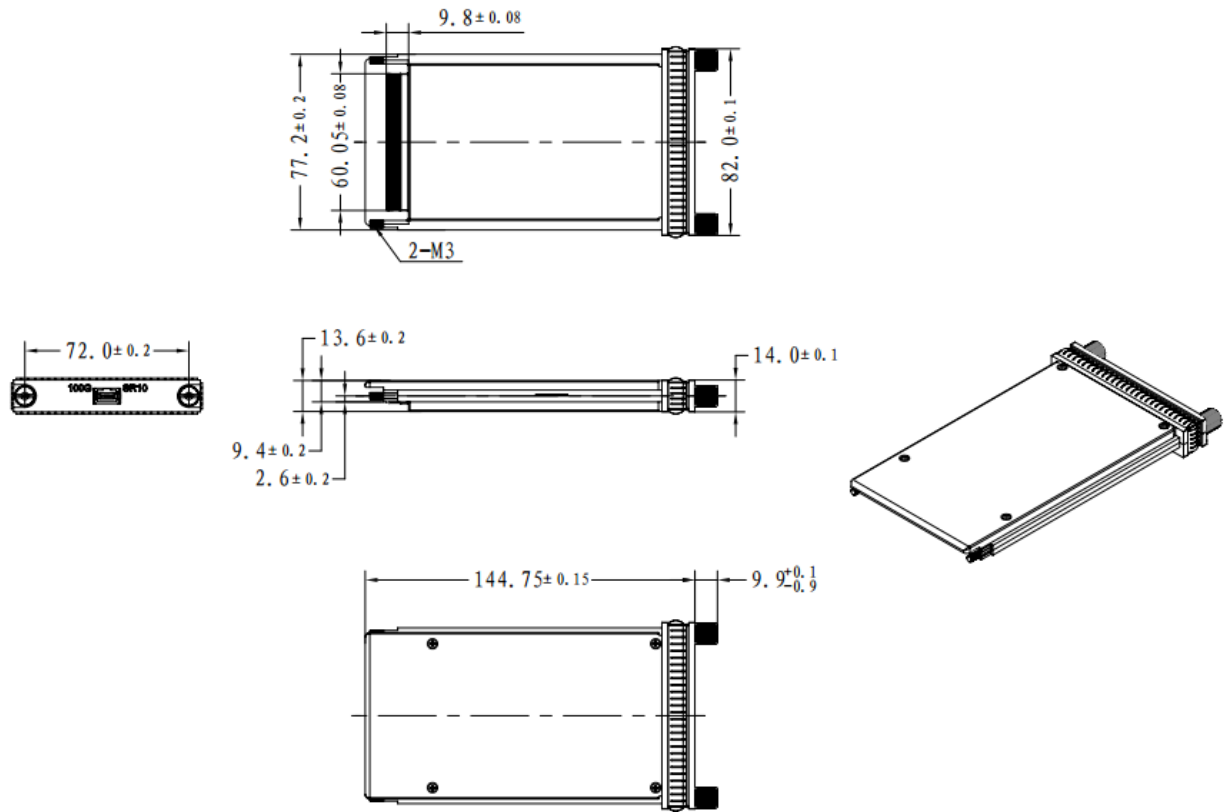
Optical interface and lanes assignment



Lanes assignment

Optical lanes	Corresponding electrical pins	Optical lanes	Corresponding electrical pins
RX0	79,80	TX0	113,114
RX1	82,83	TX1	116,117
RX2	85,86	TX2	119,120
RX3	88,89	TX3	122,123
RX4	91,92	TX4	125,126
RX5	94,95	TX5	128,129
RX6	97,98	TX6	131,132
RX7	100,101	TX7	134,135
RX8	103,104	TX8	137,138
RX9	106,107	TX9	140,141

Mechanical Specifications



Obtaining Document

You can visit our website: <http://www.eoptolink.com>

Or contact Eoptolink Technology Inc., Ltd. listed at the end of the documentation to get the latest documents.

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Michael			Preliminary.	Aug 14,2015
V1.b	Michael			Add optical interface	Feb 23,2016
V1.c	Michael			Update a slip of the pen.	May 16,2016

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Contact:

Add: Floor 5, Building 2, No. 21 Gaopeng Avenue, High-Tech District, CHENGDU, SICHUAN
610041 P.R. CHINA

Tel: (+86) 028-85122709 ext 816 or 809

Fax: (+86) 028-85121912

Postal: 610041

E-mail: sales@eoptolink.com

<http://www.eoptolink.com>