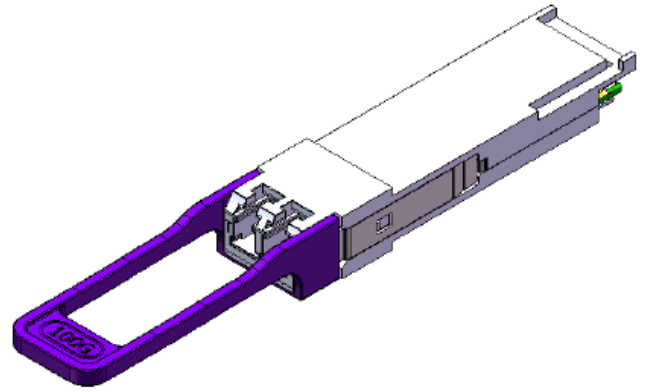


EOLQ-161HG-10-SI1 Series

Single-Mode CPRI/100GBASE CWDM4 10Km QSFP28 Transceiver
RoHS6 Compliant

Features

- ◆ Supports CPRI V7.0 Option7/8/9/10
- ◆ Supports 40Gbps/100Gbps
- ◆ Single 3.3V Power Supply
- ◆ Power dissipation < 4.5W
- ◆ Up to 10km over SMF
- ◆ RoHS-6 compliant (lead-free)
- ◆ 4x25G electrical interface
- ◆ Duplex LC receptacles
- ◆ Commercial case temperature range of
-40°C to 85°C
- ◆ 4*25Gbps DFB-based CWDM transmitter
- ◆ PIN and TIA array on the receiver side
- ◆ I2C interface with integrated Digital Diagnostic
Monitoring



Applications

- ◆ CPRI V7.0 Option7/8/9/10
- ◆ 100G CWDM4 applications with FEC

Ordering Information

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
EOLQ-161HG-10-SI1*(note1)	103Gbps	SMF	10km	LC	-40~+85°C	Yes

Note1: Standard version

Note2: Over SMF

*The product image only for reference purpose

Regulatory Compliance*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Eoptolink.

Product Description

Eoptolink's EOLQ-161HG-10-SI1 QSFP28 transceiver module is designed for use in 100 Gigabit Ethernet links over 10Km single mode fiber. They are compliant with the QSFP28 MSA, CWDM4 MSA, and portions of IEEE 802.3bm.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T _s	-45	100	°C
Supply Voltage	V _{cc}	-0.5	3.6	V
Operating Relative Humidity	RH	0	95	%
Receiver Damage Threshold, per Lane	R _x dmg	5.5		dBm

*Exceeding any one of these values may damage the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T _c	-40	25	85	°C
Power Supply Voltage	V _{cc}	3.135	3.3	3.465	V
Power Dissipation	P _D			4.5	W

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Differential data input swing per lane				900	mV _{p-p}	
Input Impedance (Differential)	Z _{in}			10	%	

Stressed input parameters					
Eye width		0.46		UI	
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13			
Eye height		95		mv	
DC common mode voltage		-350	2850	mv	
Receiver					
Differential output amplitude		200	900	mv _{p-p}	
Output Impedance (Differential)	Z _{out}		10	%	
Output Rise/Fall Time	t _r /t _f	12		ps	20%~80%
Eye width		0.57		UI	
Eye height differential		228		mv	
Vertical eye closure			5.5	dB	

Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR _{AVE}		24.33		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	λ _{C0}	1264.5		1277.5	nm
Lane_1 Center Wavelength	λ _{C1}	1284.5		1297.5	nm
Lane_2 Center Wavelength	λ _{C2}	1304.5		1317.5	nm
Lane_3 Center Wavelength	λ _{C3}	1324.5		1337.5	nm
Total Average Output Power	P _o			8.5	dBm
Average Launch Power each Lane ^{*(Note3)}	P _{each}	-4.5		2.5	dBm
Transmit OMA each Lane ^{*(Note4)}	T _{xOMA}	-2		2.5	dBm
Launch power in OMA minus TDP, each lane	OMA-TDP	-5.0			dBm
Transmitter and Dispersion Penalty per Lane ^{*(Note5)}	TDP			3	dB
Side Mode Suppression Ratio	SMSR	30			dB
-20dB Spectrum width	SW ₋₂₀			1	nm
Optical Return Loss Tolerance				20	dB
Transmitter Reflectance ^{*(Note6)}				-20	dB
Extinction Ratio	ER	3.5			dB
Average launch power of OFF transmitter, each lane	P _{off}			-30	dBm

RIN OMA	RIN			-128	dB/Hz
Eye mask definition {X1, X2, X3, Y1, Y2, Y3} ^{*(Note7)}		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			
Receiver					
Signaling Speed per Lane	BR _{AVE}		24.33		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold	Rxdmg	2.5			dBm
Lane_0 Center Wavelength	λ_{C0}	1264.5		1277.5	nm
Lane_1 Center Wavelength	λ_{C1}	1284.5		1297.5	nm
Lane_2 Center Wavelength	λ_{C2}	1304.5		1317.5	nm
Lane_3 Center Wavelength	λ_{C3}	1324.5		1337.5	nm
Average receive power ^{*(Note8)}	Rxpow	-12		2.5	dBm
Receive Power (OMA) per Lane	RxOMA			2.5	dBm
Unstressed Receiver Sensitivity (OMA) per Lane ^{*(Note9)}	Rxsens			-11.5	dBm
Unstressed Receiver Sensitivity (OMA) per Lane ^{*(Note10)}	Rxsens			-8.6	dBm
Optical Return Loss	ORL			-26	dB
Conditions of stressed receiver sensitivity test					
Vertical Eye Closure Penalty ^{*(Note11)}	VECP	1.9			dB
Stressed J2 Jitter ^{*(Note11)}	J2	0.33			UI
Stressed J4 Jitter ^{*(Note11)}	J4	0.48			UI
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3} ^{*(Note11)}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}			
LOS Assert	LOSA	-25			dBm
LOS De-Assert	LOSD			-12	dBm
LOS Hysteresis		0.5			dB

Note3: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note4: Even if the TDP < 1.0dB, the OMA (min) must exceed this value.

Note5: TDP does not include a penalty for multi-path interference (MPI).

Note6: Transmitter reflectance is defined looking into the transmitter.

Note7: Hit ratio of $5 \times 10^{-5} / 25.78\text{Gbps}$.

Note8: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note9: Sensitivity is specified at 5×10^{-5} BER /25.78Gbps.

Note10: Sensitivity is specified at 1×10^{-12} BER /25.78Gbps.

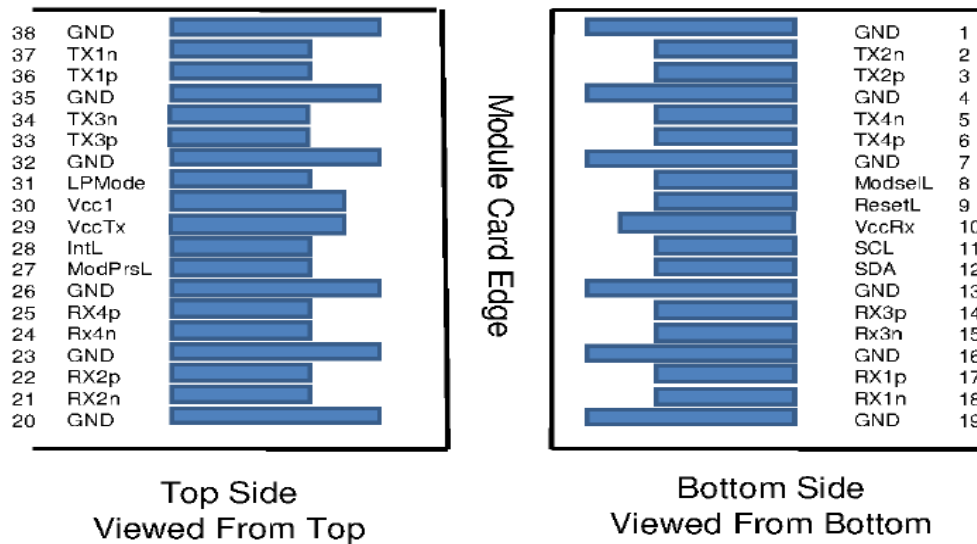
Note11: Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Rate Selection

Parameter	Per Rate	Description
CPRI line bit rate option 7	9.8304 G	Page 00H byte 98: 0x00 (Setting the CDR to OFF enables an internal bypassing mode; CDR_ON byte 98: 0xFF)
CPRI line bit rate option 8	10.1376 G	
CPRI line bit rate option 9	12.16512 G	
40GBE	10.3125 G	
CPRI line bit rate option 10	24.33024 G	CDR_ON, Page 00H bytes 87&88: 0x55
100GBE	25.78125 G	CDR_ON, Page 00H bytes 87&88: 0xAA

Note12: The default rate selection is CPRI line bit rate option 10 (per lane rate is 24.33024 G). The other rate selection by writing Reg.

QSFP28 Transceiver Electrical Pad Layout



Pin Arrangement and Definition

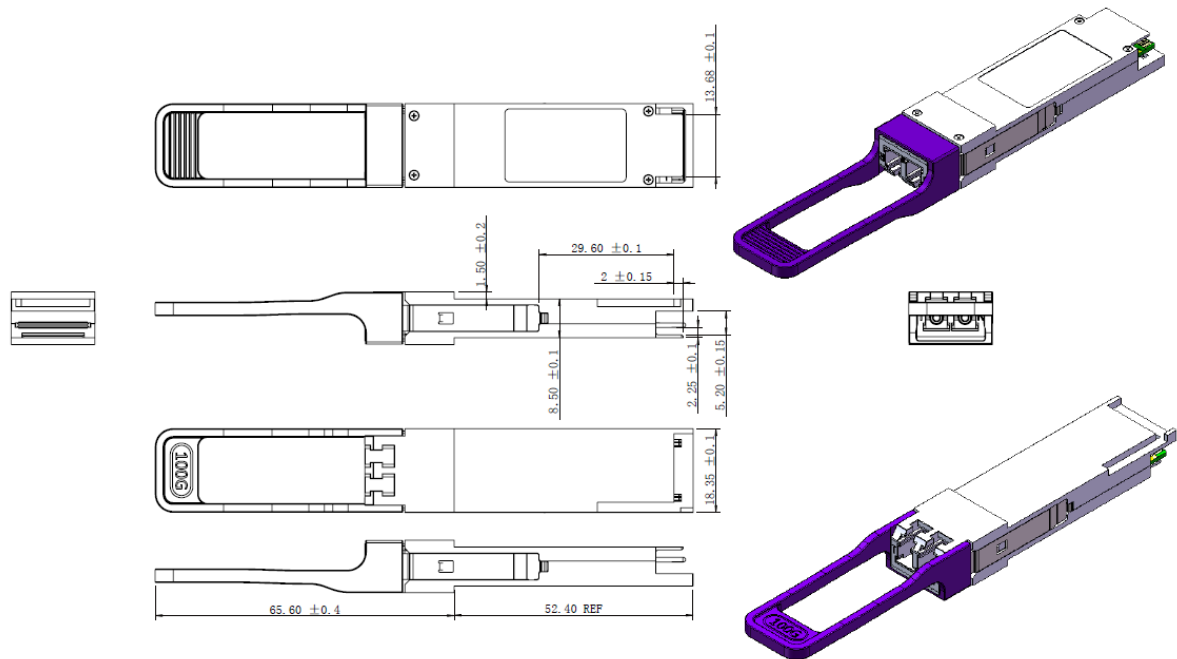
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTTL-I	ModSelL	Module Select	3	
9	LVTTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVC MOS- I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS- I/O	SDA	2-wire serial interface data	3	

13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP28 Module in any combination. The connector pins are each rated for a maximum current of 500mA.

Mechanical Specifications



*This 2D drawing only for reference, please check with Eoptolink before ordering.

Obtaining Document

You can visit our website:

Or contact Eoptolink Technology Inc., Ltd. Listed at the end of the documentation to get the latest documents.

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Rowan	Erik/Eliss/Tracy		Preliminary.	Nov 15,2017

Notice:

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